REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Applicants acknowledge with appreciation the indication in the Office Action that claim 13 is allowed and claims 4 and 5 are allowable.

Proposed changes to Figs. 1, 2, 3A-3D, 4, and 7 are submitted to overcome the objections identified in the Office Action.

The specification has been amended to overcome the objections thereto. Also, both the abstract and the specification have been amended to overcome the objection to Fig. 4, based on the conflict between the label attached to reference character 103 in Fig. 4 and that recited in the specification. No new matter has been introduced by the amendments to the drawings and specification.

Claims 1-13 have been canceled in favor of new claims 14-23, which better define the subject matter Applicants regard as the invention. Support for the features recited in claims 14-23 is provided by the original claims, Fig. 4, and the description of Fig. 4 in the specification. The new claims have been drafted to avoid the issues underlying the objections to claims 8-10.

Claims 1-3 and 6-12 were rejected, under 35 USC §102(b), as being anticipated by the Motorola article (A Proposal for Turbo Code Interleaving) (hereinafter Motorola). To the extent these rejections are deemed applicable to new claims 14-23, Applicants respectfully traverse.

Features of the presently claimed invention include a bit inversion apparatus that inverts a bit of a row number, a shift register that shifts a bit of the bit-inverted row number and outputs the result as an address offset value, and a column exchange section that outputs an address value corresponding to the bit-inverted row number and the column number as a column conversion value. With these features, the present invention generates an interleave address by adding the address offset value and the column conversion value.

The claimed structure provides the advantage of outputting row numbers and column numbers individually, converting these numbers individually, and thereby performing row rearrangement processing and column rearrangement processing in parallel. As a result, the interleave address patterns are generated in a small memory space and short processing time.

To be more specific, the interleave address generation apparatus of the present invention divides a two-dimensional array of a block interleave system into row numbers and column

numbers and processes these numbers individually. This structure solves the memory space and processing time problems existing in conventional interleave address generation systems. In a conventional system, an interleave address pattern is created in predetermined units in memory. Thereafter, a row rearrangement operation and the addition of offset addresses are applied to the pattern stored to memory. Thus, the conventional system requires considerable memory space and processing time to generate an interleave address pattern.

The present invention generates varying row rearrangement patterns (i.e., address offset value's) using the bit inverting section and the shift register and generates varying column rearrangement patterns (i.e., column conversion values) using the column exchange section.

Motorola fails to disclose or suggest a column exchange section, as recited in claim 14. Thus, Motorola's device cannot achieve the above-noted advantage of outputting a row number and a column number individually, converting these numbers individually, and thereby performing row rearrangement processing and column rearrangement processing in parallel, so as to generate an interleave address pattern within a small memory space and short processing time. Claim 23 recites the

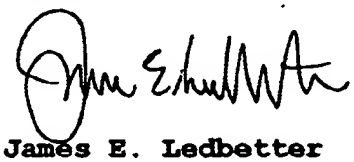
functionality provided by the column exchange section recited in claim 14, but with respect to a method claim.

Accordingly, Applicants submit that Motorola does not anticipate the subject matter defined by claims 14 and 23. Therefore, allowance of claims 14 and 23 and all claims dependent therefrom is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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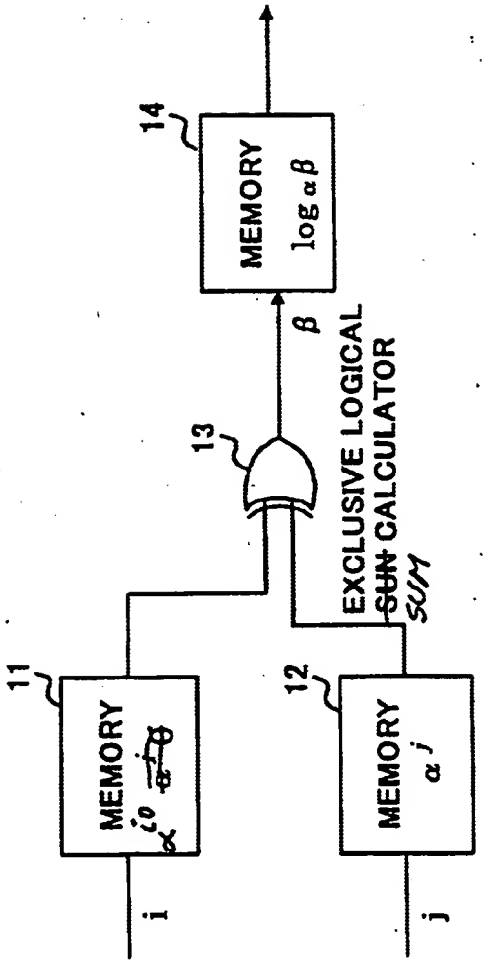

FIG.1

RELATED ART

RELATED ART

POWER EXPRESSION β	VECTOR EXPRESSION	$\log_\alpha \beta$
α^0	100	0
α^1	010	1
α^2	001	2
α^3	110	3
α^4	011	4
α^5	111	5
α^6	101	6
$\alpha^7(0)$	000	(7)

FIG.2

i \ N	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
1	6	4	7	5	1	3	0	2	2
2	4	6	3	2	0	7	1	5	5
3	5	2	1	6	7	0	3	4	4

FIG.3A
RELATED ART

i \ N	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
2	4	6	3	2	0	7	1	5	5
1	6	4	7	5	1	3	0	2	2
3	5	2	1	6	7	0	3	4	4

FIG.3B
RELATED ART

i \ N	0	1	2	3	4	5	6	7	i_0
0	7	3	6	1	5	4	2	0	0
2	20	22	19	18	16	23	17	21	5
1	14	12	15	13	9	11	8	10	2
3	29	26	25	30	31	24	27	28	4

FIG.3C
RELATED ART

[7, 20, 14, 29, 3, 22, 12, 26, 6, 19, 15, 25, 1, 18, 13, 5,
16, 9, 4, 23, 11, 24, 2, 17, 8, 27, 0, 21, 10, 28]

FIG.3D
RELATED ART

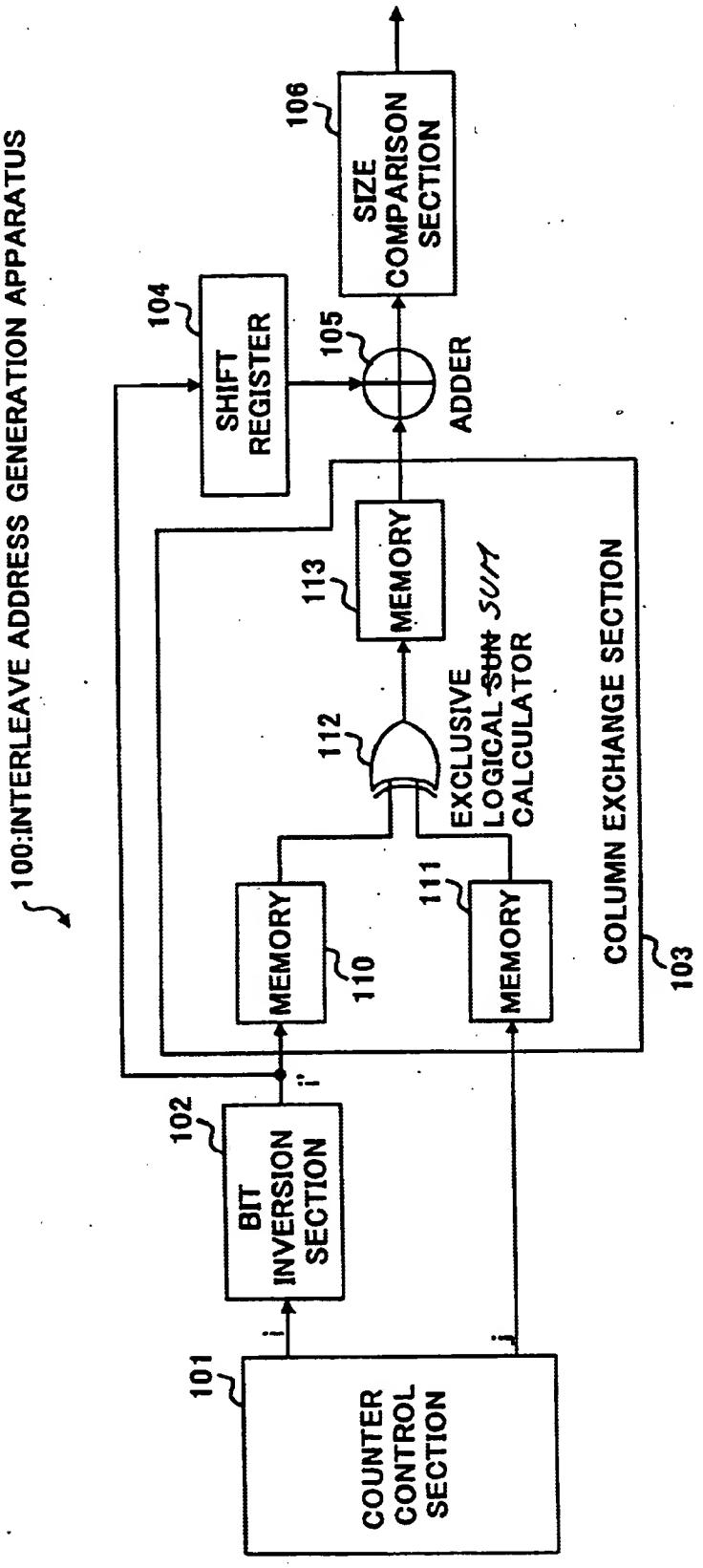

FIG.4

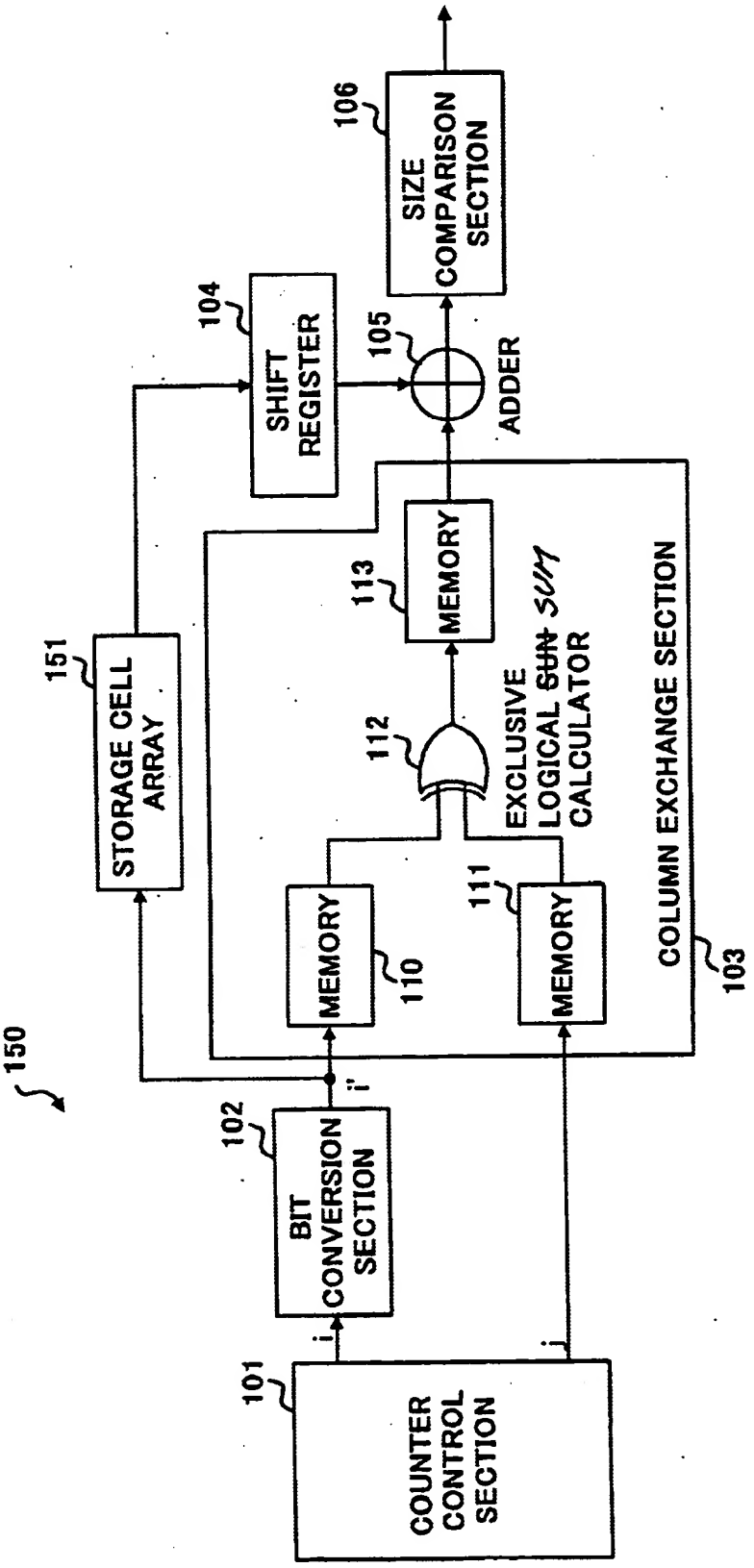

FIG.7